Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-5. (Cancelled)

6. (Currently Amended) A circuit structure, comprising:

a semiconductor substrate having thereon circuitry including high and low voltage transistors; and

a matrix of non volatile memory cells organized in rows and columns integrated on the semiconductor substrate, each memory cell having a floating gate transistor and a selection transistor, said rows being interrupted by at least a couple of byte selection transistors, said transistors being manufactured in respective active areas delimited by portions of an insulating layer, said circuit structure having a first and a second multilayer band formed on said semiconductor substrate, each band having a first gate oxide layer, a first polysilicon layer, a second dielectric layer and a second polysilicon layer, said first band defining the gate regions of said byte selection transistor and of said selection transistor in correspondence with said respective active areas and having a portion extending on a portion of the insulating layer adjacent to said byte selection transistor, said second band defining the gate regions of said floating gate transistor, wherein said portion of said first band is provided with an opening, formed in said second dielectric layer and in said second polysilicon layer, filled at least partially by a conductive layer said portion of said first band having a greater width at the location of said opening than the width at the location of said active areas.

7. (Cancelled)

8. (Previously Presented) The circuit structure according to claim 6, wherein said conductive layer is a polysilicon layer.

9. (Previously Presented) The circuit structure according to claim 6, wherein said conductive layer is a metallization layer.

10. (Currently Amended) A device, comprising:

a semiconductor substrate;

a first active region of the substrate defined by a first opening in an insulating layer formed on the substrate;

first and second transistors formed in the first active region of the semiconductor substrate;

a first portion of a multilayer structure formed, with a first width, over the first transistor and, with a second width, greater than the first width, over a region of the insulating layer, the multilayer structure including a gate oxide layer, a first polysilicon layer, a dielectric layer, and a second polysilicon layer;

a second portion of the multilayer structure formed over the second transistor, the second portion electrically separate from the first portion;

an opening formed in the dielectric layer and the second polysilicon layer of the first portion of the multilayer structure, over the region of the insulating layer; and

a conductive layer formed in the opening and electrically connecting the first and second polysilicon layers of the first portion of the multilayer structure.

11. (Previously Presented) The device of claim 10, comprising a transition layer formed between the conductive layer and the first polysilicon layer, and between the conductive layer and the second polysilicon layer.

12. (Previously Presented) The device of claim 10 wherein a region of the gate oxide layer of the second portion of the multilayer structure is a tunnel oxide region of the second transistor.

13. (Previously Presented) The device of claim 10, comprising a memory matrix of memory cells, wherein the first transistor is a selection transistor of the memory matrix and the second transistor is a floating gate transistor of the memory matrix.

14. (Previously Presented) The device of claim 13, comprising:

a second active region of the substrate defined by a second opening in the insulating layer formed on the substrate; and

a third transistor formed in the second active region, wherein the first portion of the multilayer structure is formed over the third transistor.

15. (Previously Presented) The device of claim 14 wherein the third transistor is a byte selection transistor.

16. (Previously Presented) The device of claim 15, comprising:

a first plurality of selection transistors formed on the substrate, wherein the first transistor is one of the first plurality of selection transistors, and wherein the first portion of the multilayer structure is formed over each of the first plurality of selection transistors; and

a first plurality of floating gate transistors formed on the substrate, wherein the second transistor is one of the first plurality of floating gate transistors, and wherein the second portion of the multilayer structure is formed over each of the first plurality of floating gate transistors.

17. (Previously Presented) The device of claim 16 wherein:

the memory matrix comprises a plurality of bytes arranged in rows and columns;

the first pluralities of selection transistors and floating gate transistors are components of a first one of the plurality of bytes; and

each of the plurality of bytes comprises a respective plurality of selection transistors, a respective plurality of floating gate transistors and a respective byte selection transistor.

18. (Currently Amended) A memory matrix formed on a semiconductor substrate and having a plurality of bytes arranged in rows and columns, each byte comprising:

a plurality of memory cells, each memory cell including a selection transistor and a floating gate transistor formed together in one of a plurality of active regions of the substrate;

a byte selection transistor formed in another one of the plurality of active regions of the substrate;

a first segment of a multilayer structure formed to extend, at a first width, over each of the selection transistors of the byte~~;~~ and over the byte selection transistor, and, at a second width, greater than the first width, over a portion of an insulating layer formed between two of the plurality of active regions, the ~~multiplayer~~ multilayer structure including:

a gate oxide layer formed on a surface of the substrate,

a first polysilicon layer formed on the gate oxide layer,

a dielectric layer formed on the first polysilicon layer, and

a second polysilicon layer formed on the dielectric layer;

an opening formed in the dielectric layer and second polysilicon layer in a region of the first segment extending over the portion of the insulating layer;

a conductive layer formed in the opening, electrically coupling the first and second polysilicon layers; and

a second segment of the multilayer structure formed to extend over each of the floating gate transistors of the byte.

19. (Previously Presented) The memory matrix of claim 18 wherein the second segment of the multilayer structure of each of the plurality of bytes in a same row is a common segment

20. (Previously Presented) The memory matrix of claim 18 wherein each byte comprises eight bits.